Abstract of the Disclosure:

In semiconductor memories having a surrounding gate configuration, webs, i.e. vertical rectangular pillars made of substrate material, are formed at the surface of a semiconductor substrate and are surrounded by the gate electrodes in a lower region. Conventionally, it is not possible for word lines to make contact with the gate electrodes in the lower region of the webs without at the same time electrically influencing substrate regions at a higher level in the webs or short-circuiting bit lines from their sidewalls, unless complicated methods requiring additional lithography steps are used. A method for the self-aligning, selective contact-connection of the peripheral gate electrodes is performed with the aid of an insulation layer having a smaller layer thickness than the peripheral gate electrodes.

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